Refine Search

Search Results -

Term	Documents
BUS	188221
BUSES	46947
BUSSES	16155
CONTROLLER	329016
CONTROLLERS	69719
(3 AND (BUS ADJ CONTROLLER)).USPT.	0
(L3 AND BUS ADJ CONTROLLER).USPT.	0

Database:
- US Pre-Grant Publication Full-Text Database
- US Patents Full-Text Database
- US OCR Full-Text Database
- EPO Abstracts Database
- JPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Search: L30

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Tuesday, January 18, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=ADJ			
L30	L3 and bus adj controller	0	L30
L29	L3 and controller	4	L29
L28	PCI and peer adj bus and interference and host adj bus	0	L28
L27	PCI and peer adj bus and interference and noise and host adj bus	0	L27
L26	L22 and interfer	0	L26
L25	L22 and interference	1	L25
L24	L21 and process adj bus	0	L24
L23	L21 and transaction adj bus	0	L23

L22	L21 and transaction	12	L22
L21	L20 and host adj processor	31	L21
L20	PCI adj bus and host adj bus and noise	192	L20
L19	peer adj bus and host adj bus and noise	0	L19
L18	moriarty and peer and interference	1	L18
L17	L16 and transaction adj bus	3	L17
L16	PCI and bus and interference and peer and host	69	L16
L15	L14 and host adj processor	1	L15
L14	L13 and transaction adj bus	4	L14
L13	host and peer and interference	353	L13
L12	host adj channel adj peer adj channel and interference	0	L12
L11	L10	0	L11
L10	L3 and interference	0	L10
L9	L3 and interferring	0	L9
L8	L3 and interfer	0	L8
L7	host adj transaction and peer adj transaction	0	L7
L6	peer adj transaction and host adj transaction and interference	0	L6
L5	L3 and interference	0	L5
L4	L3 and interence	0	L4
L3	L2 and host adj processor	4	L3
L2	peer adj bus and host adj bus	12	L2
L1	peer adj transaction adj bus and host adj transation adj bus	0	L1

END OF SEARCH HISTORY